Amendments to the Claims:

Claim 1. (Amended) A method of forming a structure having a textured surface for a semiconductor assembly comprising:

forming hemi-spherical grain silicon over a supporting substrate; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 2. (Original) The method of claim 1, further comprising forming an amorphous silicon layer on the supporting substrate prior to the formation of the hemi-spherical grain silicon.

Claim 3. (Original) The method of claim 2, wherein the amorphous silicon layer is formed by decomposing SiH_4 at approximately 500°C.

Claim 4. (Original) The method of claim 2, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 5. (Original) The method of claim 1, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 550 to 1000°C.

Claim 6. (Original) The method of claim 1, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 7. (Original) The method of claim 1, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 8. (Original) The method of claim 7, wherein the number of cycles performed is 5 cycles.

Claim 9. (Canceled)

Claims 10. (Amended) A method of forming a memory cell for a semiconductor assembly comprising:

forming an access transistor to a storage capacitor;

forming a conductive plug connecting to a source/drain of the access transistor;

forming hemi-spherical grain silicon on the conductive plug; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 11. (Original) The method of claim 10, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 12. (Amended) The method of claim ~~10~~ 11, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 13. (Original) The method of claim 10, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 14. (Original) The method of claim 10, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 15. (Original) The method of claim 14, wherein the number of cycles performed is 5 cycles.

Claim 16. (Canceled)

Claim 17. (Amended) A method of forming a storage node capacitor plate for a semiconductor assembly comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 18. (Original) The method of claim 17, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 19. (Original) The method of claim 17, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 800 to 1000°C.

Claim 20. (Original) The method of claim 17, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 21. (Original) The method of claim 17, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 22. (Amended) The method of claim 21, wherein the number of cycles performed is 5 ~~cycles~~ cycles.

Claim 23. (Canceled)

Claim 24. (Amended) A method of forming a capacitor structure for a semiconductor assembly during fabrication thereof comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material;

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction;

removing undesired regions of the hemi-spherical grain silicon and the epitaxial silicon to form a storage node capacitor plate;

forming a capacitor dielectric over the storage node capacitor plate; and

forming a capacitor top plate over the capacitor dielectric.

Claim 25. (Original) The method of claim 24, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 26. (Canceled)

Claim 27. (Amended) A semiconductor structure with a textured-surface for a semiconductor assembly comprising:

a hemi-spherical grain silicon on a supporting substrate; and

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 28. (Original) The semiconductor structure of claim 27, further comprising an amorphous silicon layer underlying the hemi-spherical grain silicon.

Claim 29. (Amended) The semiconductor structure of claim ~~27~~ 28, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 30. (Original) The semiconductor structure of claim 27, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 31. (Canceled)

Claim 32. (Amended) A memory cell for a semiconductor assembly comprising:

an access transistor to a storage capacitor;

a conductive plug connecting to a source/drain of the access transistor;

a hemi-spherical grain silicon overlying the conductive plug; and

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 33. (Original) The memory cell of claim 32, further comprising an amorphous silicon layer between the source/drain region of the access transistor and the conductive plug.

Claim 34. (Canceled)

Claim 35. (Amended) A capacitor plate for a semiconductor assembly comprising:

a hemi-spherical grain silicon connecting to a conductive material; and

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 36. (Original) The capacitor plate of claim 35, wherein the conductive material comprises an underlying conductive polysilicon plug.

Claim 37. (Original) The capacitor plate of claim 35, wherein the conductive material comprises an amorphous silicon layer directly connecting to an underlying conductive polysilicon plug.

Claim 38. (Amended) The capacitor plate of claim ~~35~~ 37, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 39. (Original) The capacitor plate of claim 35, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 40. (Canceled)

Claim 41. (Original) A semiconductor assembly having a capacitor structure comprising;

an isolation material having a hole therein;

a hemi-spherical grain silicon residing in the hole and connecting to a conductive material;

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon is an oblong silicon shape that has more thickness in the vertical direction that graduates down to less thickness in the horizontal direction;

a capacitor dielectric overlying the epitaxial silicon; and

a capacitor plate overlying the capacitor dielectric.

Claim 42. (Original) The semiconductor assembly of claim 41, wherein the conductive material comprises an underlying conductive polysilicon plug.

Claim 43. (Original) The semiconductor assembly of claim 41, wherein the conductive material comprises an amorphous silicon layer directly connecting to an underlying conductive polysilicon plug.

Please add claims 44-80 as recited below.

Claim 44. (New) A method of forming a structure having a textured surface for a semiconductor assembly comprising:

forming hemi-spherical grain silicon over a supporting substrate; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 45. (New) The method of claim 44, further comprising forming an amorphous silicon layer on the supporting substrate prior to the formation of the hemi-spherical grain silicon.

Claim 46. (New) The method of claim 45, wherein the amorphous silicon layer is formed by decomposing SiH_4 at approximately 500°C.

Claim 47. (New) The method of claim 45, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 48. (New) The method of claim 44, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 550 to 1000°C.

Claim 49. (New) The method of claim 44, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 50. (New) The method of claim 44, wherein the number of cycles performed is 5 cycles.

Claim 51. (New) The method of claim 44, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 52. (New) A method of forming a memory cell for a semiconductor assembly comprising:

forming an access transistor to a storage capacitor;

forming a conductive plug connecting to a source/drain of the access transistor;

forming hemi-spherical grain silicon on the conductive plug; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 53. (New) The method of claim 52, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 54. (New) The method of claim 53, wherein the amorphous silicon layer has a thickness of about 200 to 500Angstroms.

Claim 55. (New) The method of claim 52, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 56. (New) The method of claim 52, wherein the number of cycles performed is 5 cycles.

Claim 57. (New) The method of claim 52, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 58. (New) A method of forming a storage node capacitor plate for a semiconductor assembly comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber.

Claim 59. (New) The method of claim 58, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 60. (New) The method of claim 58, wherein the hemi-spherical grain silicon is formed by decomposing DCS ($Si_2H_2Cl_2$) in an H_2 and HCl environment at about 800 to 1000°C.

Claim 61. (New) The method of claim 58, wherein the epitaxial silicon thickness is approximately 100Angstroms.

Claim 62. (New) The method of claim 58, wherein the number of cycles performed is 5 cycles.

Claim 63. (New) The method of claim 58, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 64. (New) A method of forming a capacitor structure for a semiconductor assembly during fabrication thereof comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material;

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the grain size of the epitaxial silicon is controlled by the number of cycles performed in a deposition chamber, with each cycle performed at a temperature of approximately 750-900°C and further comprising:

flowing approximately 5-50sccm of Si_2H_6 for approximately 5-20seconds followed by a first evacuation of the chamber;

flowing approximately 1-20sccm of Cl_2 for approximately 5-20seconds followed by a second evacuation of the chamber; and

flowing approximately 10-100sccm of H_2 for approximately 5-20seconds followed by a third evacuation of the chamber;

removing undesired regions of the hemi-spherical grain silicon and the epitaxial silicon to form a storage node capacitor plate;

forming a capacitor dielectric over the storage node capacitor plate; and

forming a capacitor top plate over the capacitor dielectric.

Claim 65. (New) The method of claim 64, further comprising an amorphous silicon layer formed between the source/drain region of the access transistor and the conductive plug.

Claim 66. (New) The method of claim 64, wherein the epitaxial silicon forms an oblong silicon shape that has more thickness in a vertical direction that graduates down to less thickness in a horizontal direction.

Claim 67. (New) A method of forming a semiconductor assembly having a textured surfaced structure comprising:

forming hemi-spherical grain silicon over a supporting substrate; and

forming epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon has a non-uniform thickness across the outer surface of the hemi-spherical grain silicon.

Claim 68. (New) The method of claim 67 wherein the non-uniform thickness across the outer surface of the hemi-spherical grain silicon forms an oblong outer surface of the epitaxial silicon.

Claim 69. (New) The method of claim 67, wherein the epitaxial silicon thickness varies in thickness up to approximately 100Angstroms.

Claim 70. (New) The method of claim 67, wherein the textured surfaced structure is a capacitor structure.

Claim 71. (New) A method of forming a semiconductor assembly having textured surfaced structure comprising:

forming hemi-spherical grain silicon directly connecting to an underlying conductive material;

forming epitaxial silicon directly on an outer surface of the hemi-spherical grain silicon, wherein a thickness of the epitaxial silicon varies across the surface of the hemi-spherical grain silicon such that the epitaxial silicon has a greatest thickness at an apex of the hemi-spherical grain silicon.

Claim 72. (New) The method of claim 71, wherein the textured surfaced structure is a capacitor structure.

Claim 73. (New) The method of claim 71, wherein the epitaxial silicon thickness varies in thickness up to approximately 100Angstroms.

Claim 74. (New) A semiconductor assembly having a textured surfaced structure comprising:

a hemi-spherical grain silicon over a supporting substrate; and

an epitaxial silicon directly on the hemi-spherical grain silicon, wherein the epitaxial silicon has a non-uniform thickness across the outer surface of the hemi-spherical grain silicon.

Claim 75. (new) The semiconductor assembly of claim 74, wherein an outer surface of the epitaxial silicon is oblong shaped.

Claim 76. (New) The semiconductor assembly of claim 74, wherein the epitaxial silicon thickness varies in thickness up to approximately 100Angstroms.

Claim 77. (New) The semiconductor assembly of claim 74, wherein the textured surfaced structure is a capacitor structure.

Claim 78. (New) A semiconductor assembly having textured surfaced structure comprising:

A hemi-spherical grain silicon directly connecting to an underlying conductive material; and

an epitaxial silicon directly on an outer surface of the hemi-spherical grain silicon, wherein a thickness of the epitaxial silicon varies across the surface of the hemi-spherical grain silicon such that the epitaxial silicon has a greatest thickness at an apex of the hemi-spherical grain silicon.

Claim 79. (New) The semiconductor assembly of claim 78, wherein the textured surfaced structure is a capacitor structure.

Claim 80. (New) The semiconductor assembly of claim 78, wherein the epitaxial silicon thickness varies in thickness up to approximately 100Angstroms.